UM10178

25 Amp LFPAK demonstration board

Rev. 2.0 — 16 February 2011 **User manual**

Document information

Info	Content
Keywords	LFPAK, Point of Load, demonstration board
Abstract	The 25A LFPAK demonstration board is a single phase buck converter design to demonstrate the performance of NXP NextPower LFPAK MOSFETS in a small form factor point of load (POL) circuit. The 3.3 cm x 6.1 cm (1.3x2.4 inch), four layer board converts 12V nominal input to 1.2 V nominal output and is capable of output currents of 25 amps while maintaining case temperatures at or below 90 °C with a minimal 200 LFM of airflow at 25 °C ambient. Efficiencies above 90% are achieved (12v in, 3.3v out), on this small demonstration board due to the superior level of on-resistance and thermal performance of the small S08 foot print NXP NextPower LFPAK devices..

Revision history

Rev	Date	Description
v 2.0	20110216	Document changed to comply with the new identity guidelines of NXP Semiconductors.
v 1.0	20060302	Initial version

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1. Introduction

The LFPAK demo board demonstrates the performance of NXP LFPAK MOSFETS in an operational single-phase buck converter on a small 3.3cm x 6.1 cm board. The innovative SOT669 LFPAK (Loss Free PacKage) has the compact footprint of the SO8 and enables a superior level of on-resistance and thermal performance by using an underside thermal pad electrically connected to the drain.

The simple, low cost board is designed for operation from an input voltage of 12V nominal, but is capable of operation from 5V to 13V. As furnished, the board output voltage, V_{out}, is set to 1.2V. V_{out} can be adjusted from 0.8V to 5V by changing a resistor on the board. The LFPAK devices used as examples on this board are the PH5525L for the control MOSFET and PH2525L for the synchronous MOSFET. The MOSFETs are rated at 25V and have max R_{dson} resistances of 5.5 mohm and 2.5 mohm respectively (at VGS of 10V). For detailed specifications, refer to the respective MOSFET data sheets. The demo board may have different MOSFETs that represent the latest NXP NextPower MOSFET technology.

Fig 1 shows the FET footprint utilized on this board. The footprint is compatible with SO8 devices allowing SO8 packages to be used on this board if desired.

The TI TPS40077 controller was selected for its feature set which includes: voltage operating range of 4.5V to 28V, high side current limit, source and sink drivers, and anti-cross conduction protection. For controller technical information, see the TI data sheet for the TPS40077.

The board was designed as a simple low cost 25A reference design and is not intended to demonstrate the maximum performance achievable from the chosen LFPAK devices. The LFPAK devices on this board can be implemented in designs to achieve even greater output currents and efficiencies if board design and component selection (such as using a PWM controller with external high performance drivers) allow it.

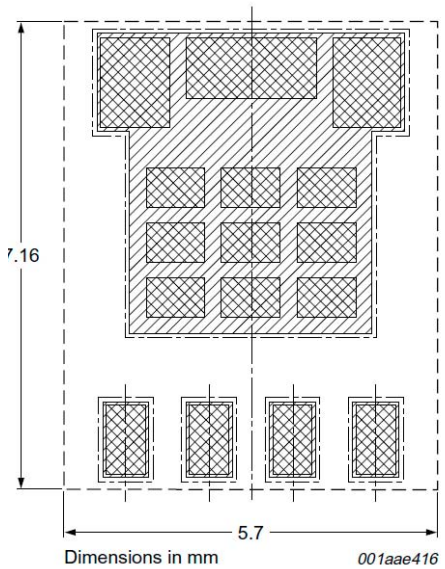

Fig 1. Simplified outline

1.1 Board Top & Bottom Views

Fig 2 shows the top and bottom view of the board. All components are located on the topside and clearance between components is arranged so attaching meters and probes is convenient. Power input connections, power output connections, and mounting hole pads are mirrored top and bottom.

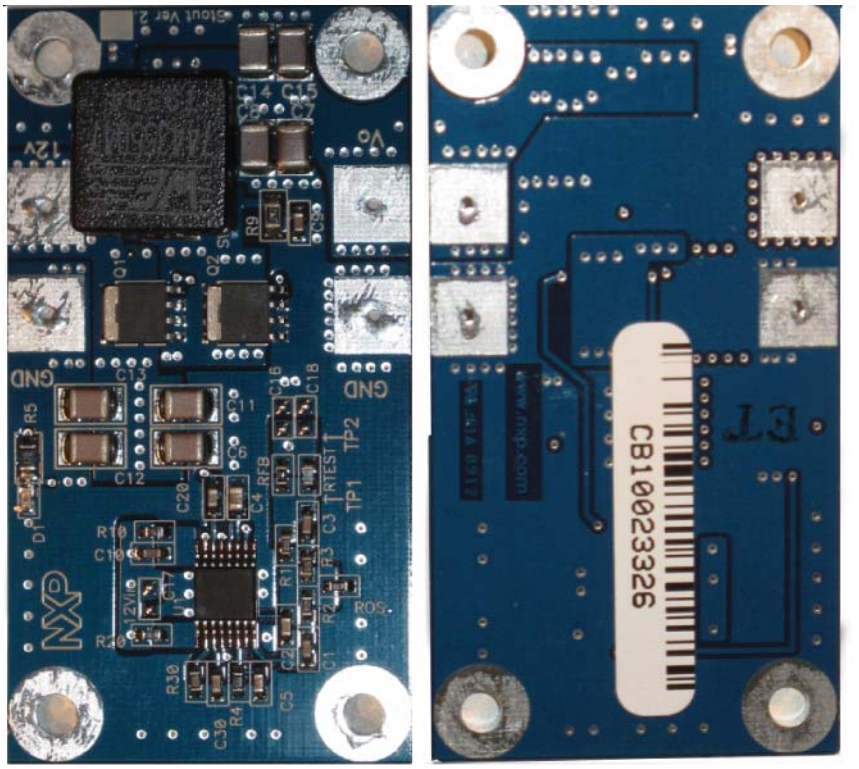

Fig 2. Top and bottom board views

1.2 Connection Details

Fig 3 shows the board connections. Input power and ground connection pads are at the top of the board, and output power and ground connection pads at the bottom. The pads are large and mirrored on the board top and bottom side for current handling capability. Solder connections or alligator clips can used to make the power attachment. Soldering to the connections pads will reduce the voltage drop of the connection. Small holes in the input and output pads are sized so conductive posts can be inserted for oscilloscope and meter probes. Mounting holes in the corners of the board are connected to power ground.

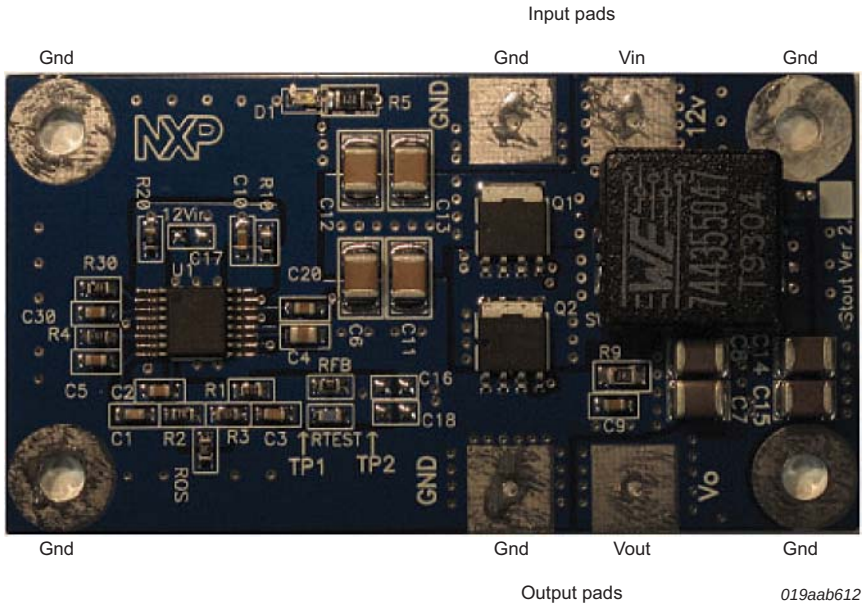

Fig 3. Input and output pads

2. Design Criteria

As supplied, the board is designed to provide an output voltage of 1.2V and 25A, but the output voltage can be changed by replacing a resistor as explained below. The current limits are also set for operation at 1.2 V. The operating frequency is set to 500 kHz. A blue status LED at the top of the board lights when the controller and board are operational. The 400nH inductor is a 30A device, (100°C), with a soft saturation curve, and was selected to provide good efficiency due to its low 0.9 mohm DCR.

2.1 Board Features

As mentioned above, output voltage can be easily adjusted by changing the value of a single resistor. The current limit can be adjusted, as described in Section 2.1.2 and will need to be altered, when adjusting the board $V_{out,}$ if a constant current limit is to be maintained. The feedback path has been designed so that phase-gain testing can be performed by removing a single resistor. A brief description these features are provided below.

2.1.1 V_{out} selection

Replacing Ros with the values calculated in the equation below changes V_{out}.

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$$Ros = R1 * Vs / (V_{out} – Vs)$$

Where Vs is the op amp reference voltage, and is fixed at 0.7V for the TPS40077. Resistor values for common output voltages are provided in Fig 4.

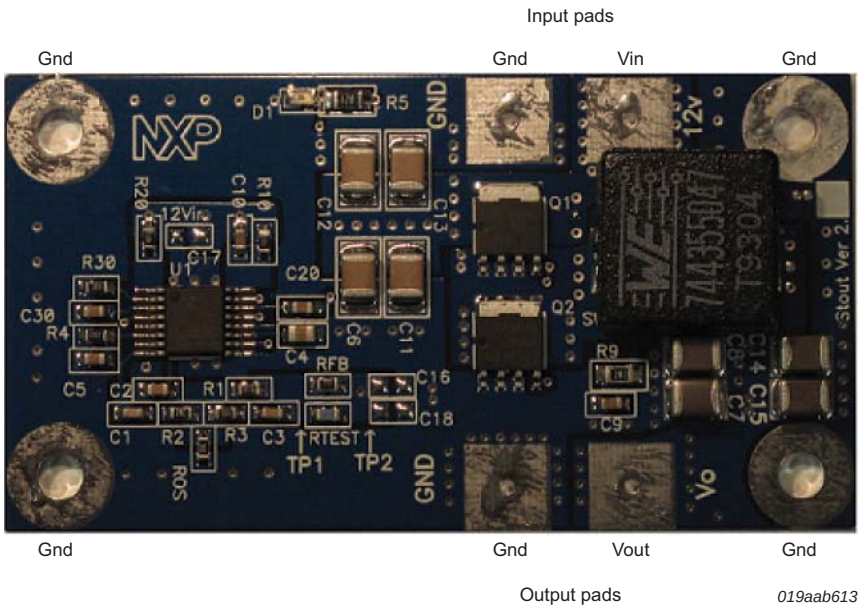


Fig 4. ROS Versus Vout

2.1.2 Control FET Current Limit

The TPS40077 data sheet discusses the parameters affecting the value of R10 for a desired current limit. The voltage drop across R10 is compared with the voltage drop across the control FET R_{dson} at full conduction, and initiates a shut down if the FET exceeds V_{R10}. The FET voltage drop is affected by the nominal values of Vout/Vin, temperature, and output current. FET voltage drop is a direct function of Rdson, and thus temperature dependent. The blue LED will flicker during cycle-to-cycle shutdown. Please see the TPS40077 data sheet for additional information on current limit settings.

The demo board is shipped with R10 equal to 1180ohms, typically initiating a cycle-to-cycle shutdown for currents exceeding 25A, (case temperatures ≤90 degC, Vin equal 12v). For other Vout and Vin values, R10 changes to provide this thermal protection. Table 1 should assist in the selection. Note that there is variation in shutdown current between demo boards, because of variation in R_{dson} between FETS.

Table 1. Shutdown current limit

Vout	Ros	R10 for Vin = 12V	R10 for Vin = 10V	R10 for Vin = 8V	Shutdown Iout
0.8V	60.4K	634	832	1180	28A
1.2V	12.1K	1180	1540	1904	25A
1.5V	7.32K	1400	1820	2260	22A
2.5V	3.32K	2370	2670	2740	22A
3.3V	2.32K	2940	3090	3090	22A
5.0V	1.40K	2610	2610	2610	20A

[1] Table note wide

a) Table note wide (level 2)

2.1.3 Phase Gain Testing

Phase gain testing (Bode plots) can be performed by removing the zero ohm RFP resistor and injecting a test signal across RTEST, a 50 ohm resistor as shown in Fig 5. By monitoring the response at TP2 to the injected signal at TP1, a phase gain plot can be generated by varying the frequency of the test signal. The full details of this test are beyond the scope of this manual, but the measurements are easily done using a Vector Network Analyzer (VNA). Please refer to the TPS40077 data sheet for loop compensation techniques. The zero ohm RFP resistor should remain in the circuit for normal operation.

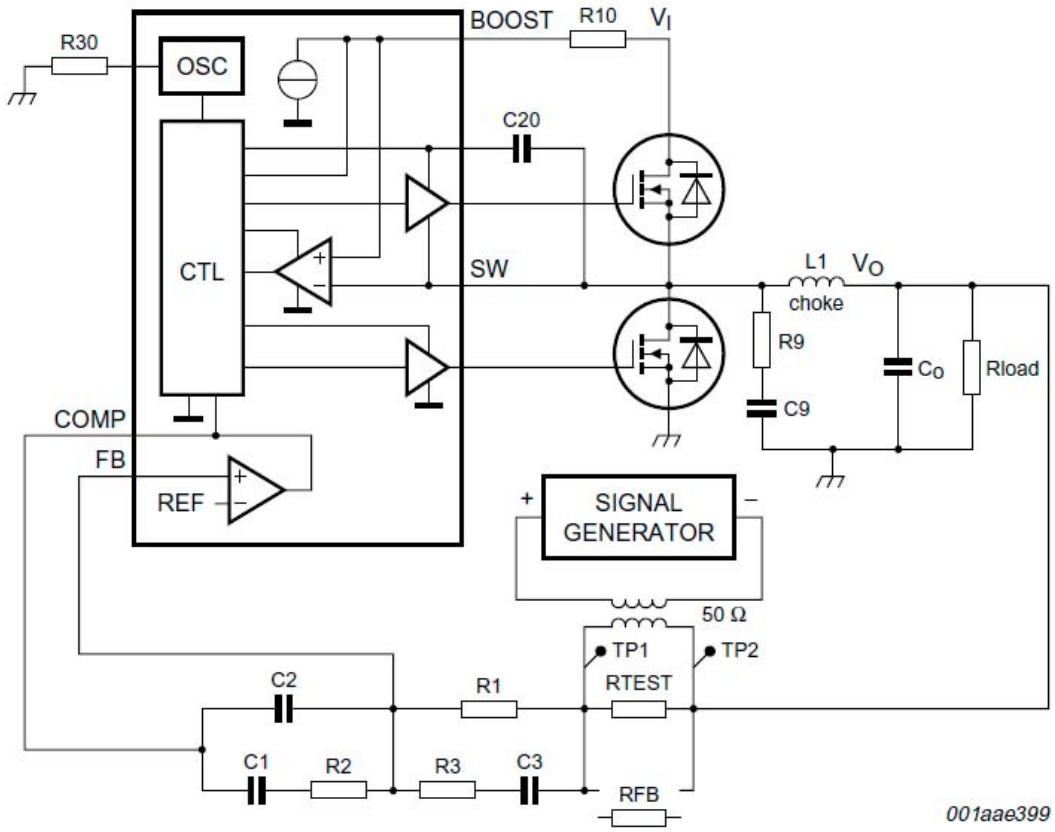


Fig 5. Phase-Gain Test Setup

2.2 Board Schematic

The board schematic is shown in Fig 6

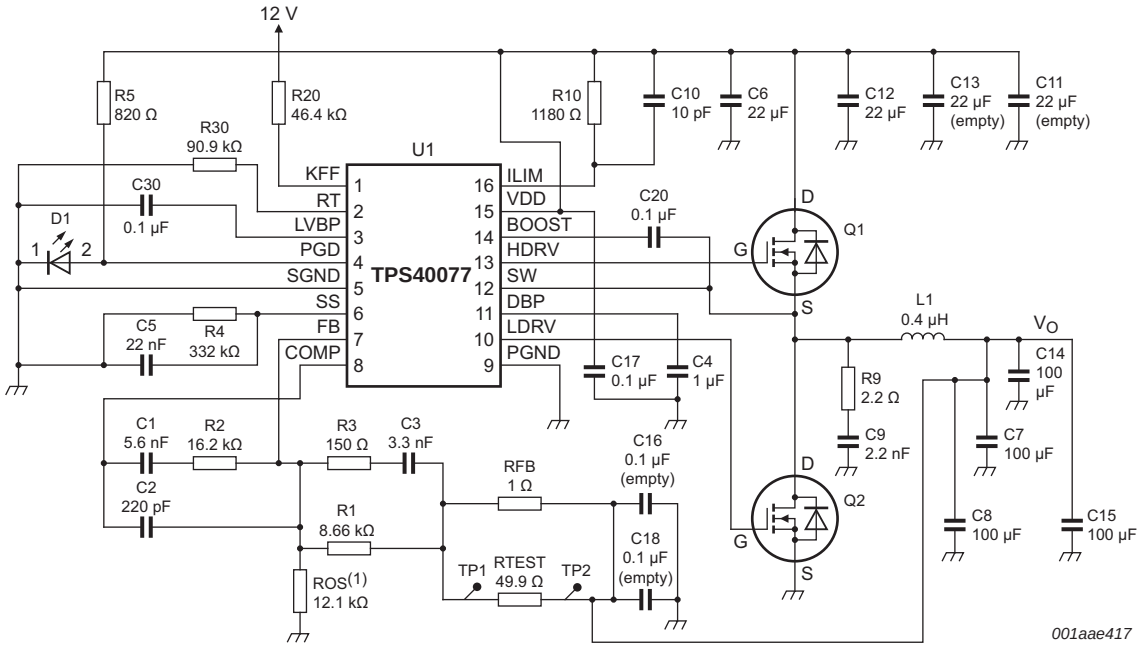


Fig 6. Schematic of the board

2.3 Layout

The demo board is four layers, all layers plated with one-ounce copper. All signals are routed top and bottom, with the inner layers servicing power and ground as shown in Fig 7. The board was designed to minimize high current induced noise in the input drive and controller circuit areas. The input current flows in a tight loop between the input pads, the input decoupling caps, and the MOSFETs. The output current is also confined to a separate loop. The controller is placed outside either of these high noise power paths. Power plane spits separate high current paths from sensitive circuit areas. The ground plane is not split and uses component placement to keep noise from the switching current out of sensitive circuit areas.

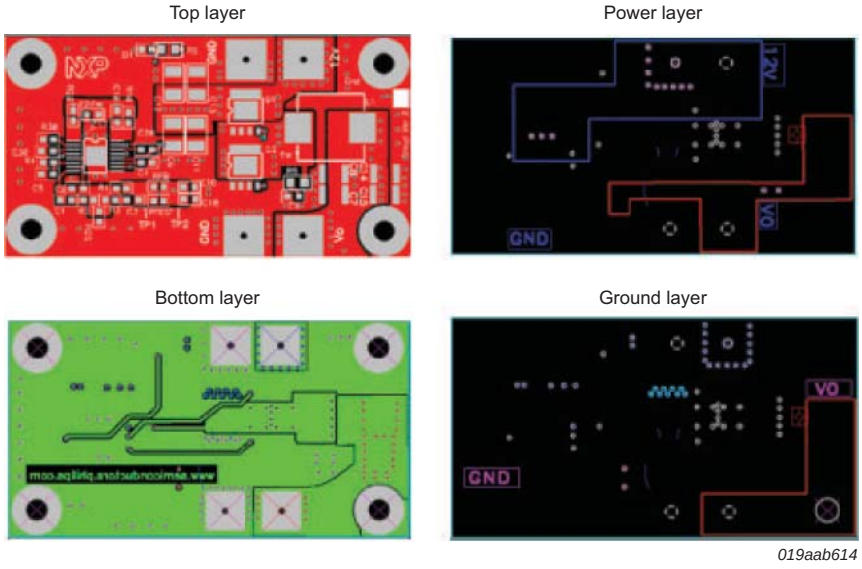


Fig 7. Board layouts

3. Electrical & Thermal Performance

The typical demo board, as designed, is capable of output currents of 25A with V_{out} set to 1.2V (30W) and 23A with V_{out} set to 3.3V (76W). This rating is based on a 90°C board temperature limit at 25°C ambient and airflow of 200LFM.

3.1 Efficiency Sweeps

Efficiency is plotted in Fig 8for V_{out} voltages of 1.2V and 3.3V. The input voltage is 12V for both sweeps. The maximum current swept is the level that produces 90°C FET case temperatures. Higher currents can be achieved with greater airflow. The current limit set point will need to be adjusted by changing R10 if higher currents are desired.

For a constant current output, the power output increases directly with V_{out}. The loss factors do not increase nearly as fast, making conversion to higher V_{out} values more efficient than conversion to lower V_{out} values.

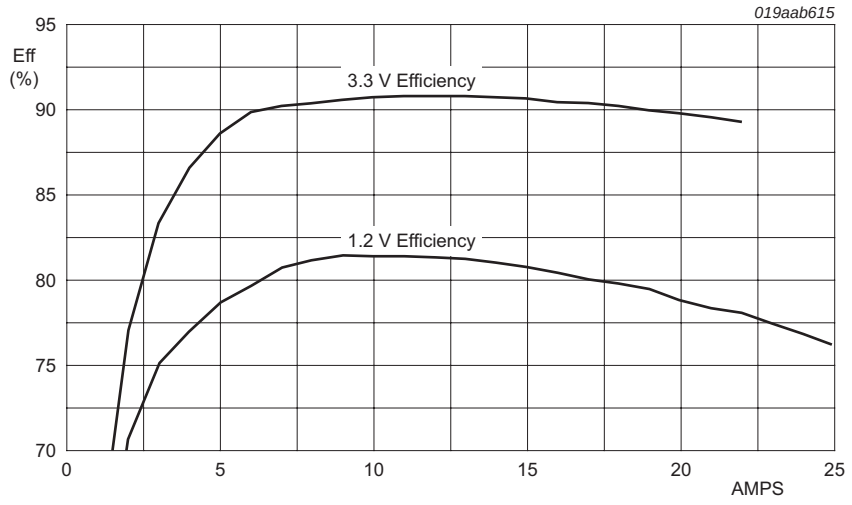
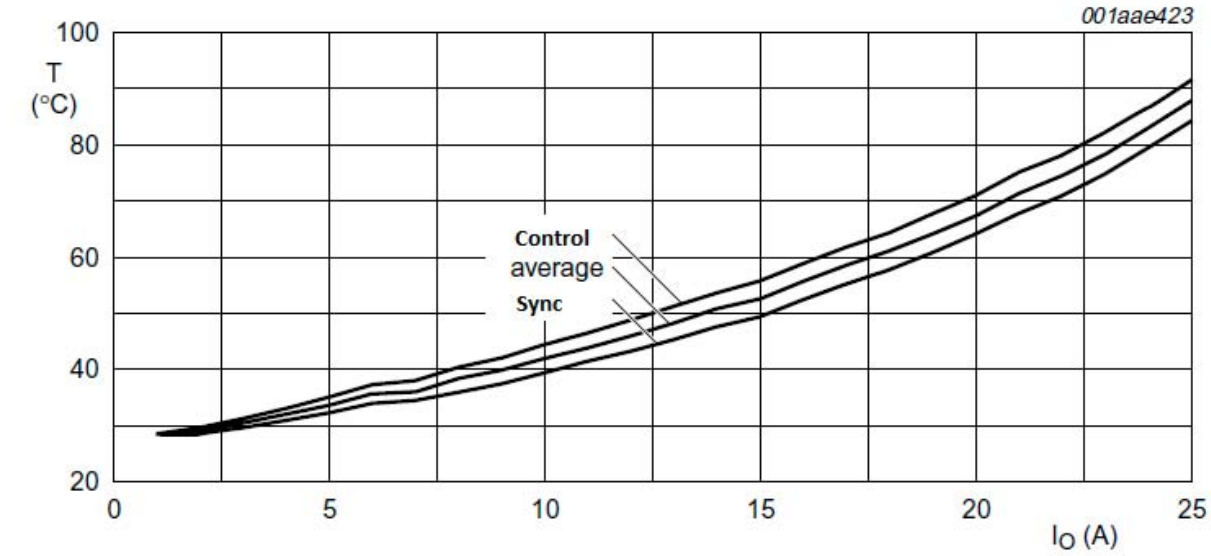


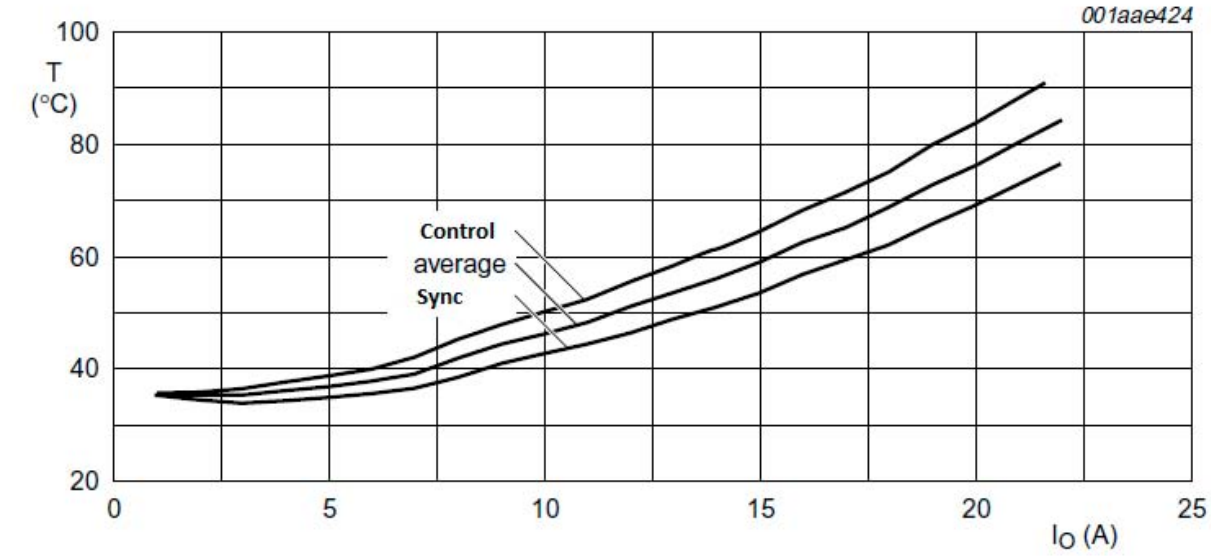
Fig 8. Efficiency sweeps 1.2V and 3.3V

3.2 Thermal Sweeps

Fig 9 show the thermal case temperature of the control and sync FETs for the efficiency sweeps in Figure 8. The load current is swept from zero amps to a maximum level, which is defined when the average of the two case temperatures equals 90^{o}C.



a. V_O = 1.2 V

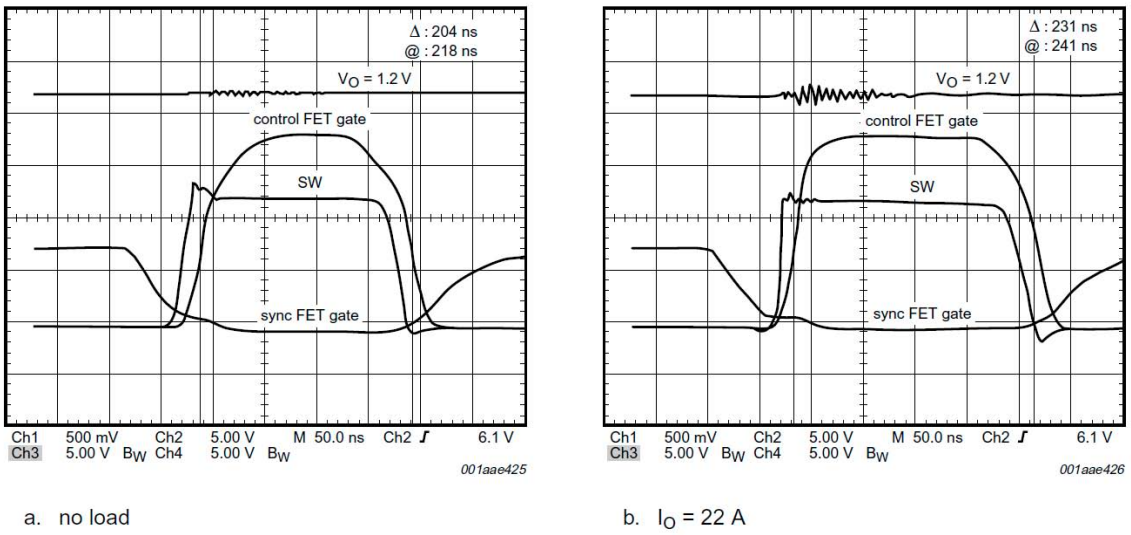


b. V_O = 3.3 V

Fig 9. Thermal measurement for 12V in

3.3 Electrical Waveforms

The oscilloscope plot in Fig 10 show the sync FET gate, control FET gate, switch Node, for a no load and a 22 Amp load respectively.



a. no load

b. I_O = 22 A

Fig 10. Waveforms at no load

3.4 Loop Gain Phase Plot

Fig 11 shows the loop gain and phase vs. frequency for V_{out}=1.2V. The compensation was very nearly the same for V_{out} ranges of 0.8V to 3.3V. The test setup is shown in Fig 5 of this manual.

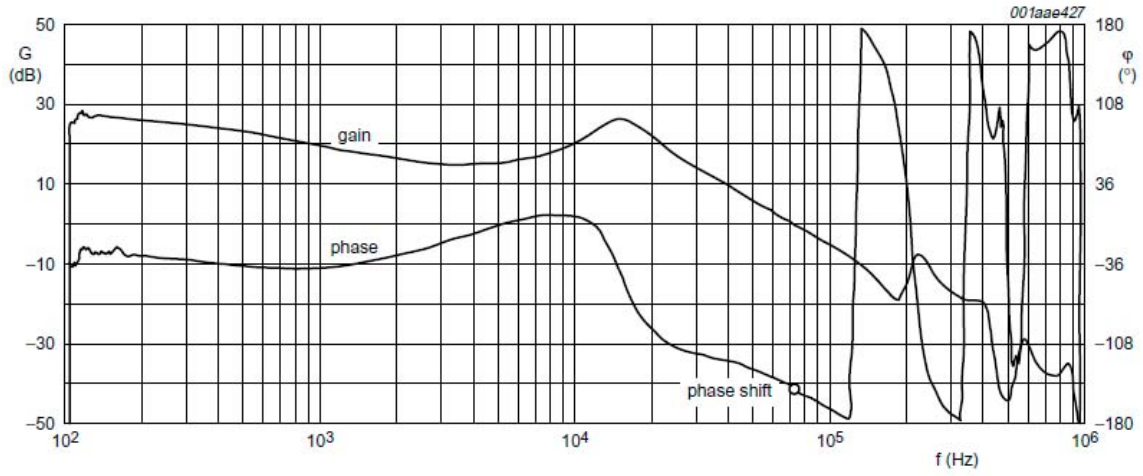


Fig 11. Phase gain plot of demonstration board

4. Bill of Materials

Table 2. LFPAK demo board BOM

Item	Qnt	Value	Package	Tolerance	Rating	Manuf	Manuf P/N	Designation
1	1	3.3nF	603	±10%	50V	TDK		C3
2	1	10pF	603	±10%	50V	TDK		C10
3	1	220pF	603	±10%	50V	TDK		C2
4	1	2.2nF	603	±10%	50V	TDK		C9
5	1	22nF	603	±10%	50V	TDK		C5
6	1	5.6nF	603	±10%	50V	TDK		C1
7	5	0.1uF	603	±10%	50V	TDK		C12, C20, C30, (C16, C18 empty)
8	1	1uF	805	±10%	16V	TDK		C4
9	4	22uF	1210	+80%, -20%	16V	TDK		C6, C12, (C11, C13 empty)
10	4	100uF	1812	+80%, -20%	6.3V	TDK		C7, C8, C14, C15
11	1	90.9k	603	±1%				R30
12	1	8.66k	603	±1%				R1
13	1	332k	603	±1%				R4
14	1	1180	603	±1%				R10
15	1	16.2k	603	±1%				R2
16	1	12.1k	603	±1%				ROS
17	1	46.4k	603	±1%				R20
18	1	150	603	±1%				R3
19	1	49.9	603	±1%				RTEST
20	1	2.2	805	±5%				R9
21	1	820	805	±5%				R5
22	1	1	603	±1%				RFB
23	1	TPS40077	SOP			TI	TPS40077PWP	U1
24	1	Control	LFPAK			NXP	Control	Q1
25	1	Sync	LFPAK			NXP	Sync	Q2
26	1	Blue LED	603		3.8V	Lite-On	LTST-C190UBKT	D1
27	1	744355047	WE-HC/HCA 13x13	±20%	0.47uH, 26A	WÜRTH	744355047	L1

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